X-Band 0.5, 1, and 2 Watt Power Amplifiers with Marked Improvement in Power-Added Efficiency

RONALD D. BOESCH, MEMBER, IEEE, AND JOYCE A. THOMPSON, MEMBER, IEEE

Abstract—**Very efficient X-band MESFET power amplifiers showing greater power-added efficiency over a wider bandwidth than any X-band amplifiers of comparable output reported to date have been designed, fabricated, and measured. The amplifiers were designed with attention to optimum bias, proper harmonic termination, and efficient power combining. This paper discusses these device and design issues, and describes a straightforward design method which achieved the increased levels of efficiency.**

I. INTRODUCTION

THE DESIGN of efficient power amplifiers requires attention to many issues. Four key elements were addressed in designing the 20% bandwidth X-band amplifiers reported here. One issue is the quiescent bias chosen for an efficient power amplifier. The bias involves a trade-off between drain efficiency and gain per stage. An important consideration for amplifiers operating in X-band and above is that the best power-added efficiency (PAE) may not occur at the lowest quiescent current bias. A second concern involves efficiency enhancement by the proper termination of the second harmonic generated by the device and whether this can be effectively accomplished over a 20% bandwidth. Yet a third issue involves the trade-off between the size of the elemental MESFET and the levels of combining required to reach a given output power level. Larger devices (which require less power combining) present increasingly difficult input matches over given bandwidths. Added levels of combining degrade efficiency as output power is lowered through combiner loss.

The final problem involves the decision of whether isolation in the output power combiner is required. The need for isolation is dependent upon the degree of similarity of parallel devices on an MMIC chip, or how well devices in a hybrid amplifier can be matched. Isolation, when required, constrains the layout of the amplifier and increases the size.

Manuscript received April 17, 1989; revised January 22, 1990.

R. D. Boesch is with the Watkins-Johnson Company, 3333 Hillview Avenue, Palo Alto, CA 94304.

J. A. Thompson was with the Watkins-Johnson Company, 3333 Hillview Avenue, Palo Alto, CA 94304. She is now with TEMAC, 222/1 Rama 9 Road, Bangkok, Thailand.

IEEE Log Number 9034916.

To investigate these issues, three very efficient single-stage hybrid amplifiers with harmonic termination and with varied levels of power combining were fabricated with 1200 (one MESFET), 2400 (two MESFET's) and 4800 (four MESFET's) μm of gate periphery. The average power-added efficiencies measured for these amplifiers were 65%, 53%, and 45% for 0.5, 1, and 2 W power levels, respectively. These amplifiers are significantly more efficient than any circuits reported to date with comparable power levels and smaller bandwidths in X-band.

II. DESIGN

The design process began with consideration of the elemental device size to be used in a unit cell and subsequent measurements on the device to obtain design information. A 1200 μm MESFET was chosen as the largest MESFET with acceptable input match for a hybrid amplifier unit cell having 20% bandwidth (see Fig. 1(a)). A larger unit cell periphery might be usable in an MMIC power amplifier of the same bandwith if prematching of 1200 μm of MESFET periphery were done first. Prematching is not as useful for hybrid amplifiers because of the size of the matching elements.

A description of the unit cell device used in this study follows. The 0.5 μm$\times$1200 μm recessed-gate GaAs MESFET's used (WJ F1200HP) were fabricated on a pulse-doped MBE structure [1] grown at the Watkins–Johnson Company. The epitaxial structure is shown in Fig. 2. On an undoped LEC GaAs substrate, the following GaAs layers were grown: p^- buffer (5000 Å), 6×10^{17} cm^{-3} Si-doped (300 Å), 1×10^{17} cm^{-3} Si-doped (700 Å), and 2×10^{18} cm^{-3} Si-doped (1000 Å).

The 0.5 μm$\times$1200 μm gate MESFET's were fabricated with 12 gate fingers by conventional recessed-gate processing. The 0.5-μm-long aluminum/titanium gates were defined by an optical lithography process having high yield and excellent uniformity [2], [3]. Devices were passivated with 1000 Å of silicon nitride and stabilized with a 300°C anneal. Au bonding pads 6 μm thick and air bridges were plated on top of evaporated Ti/Pt/Au overlay metal.

Typical dc transfer data for a 0.5 μm$\times$200 μm test MESFET are shown in Fig. 3. The plot shows drain

0018-9480/90/0600-0707$01.00

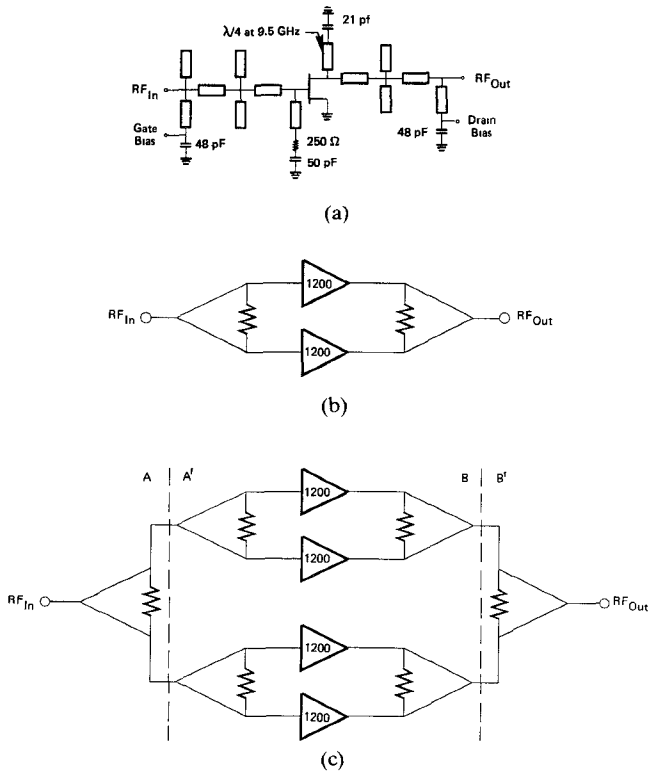


Fig. 1. Circuit schematics for the amplifiers: (a) 1200 μm unit cell amplifier; (b) 2400 μm combined amplifier; (c) 4800 μm combined amplifier showing separation planes for combiner measurement.

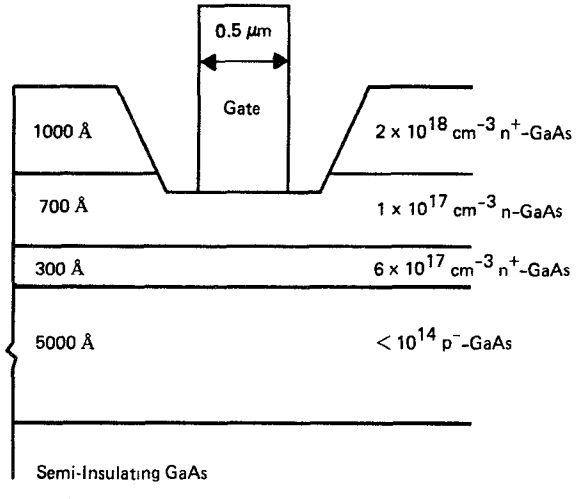


Fig. 2. Pulse-doped epitaxial structure on which GaAs MESFET's used in this study were fabricated.

current (I_{ds}) and transconductance (g_m) versus gate voltage (V_g). Note that g_m slightly increases as the FET is pinched off and reaches a maximum at about 30% of the saturated drain current (I_{dss}). At this point, the ratio of g_m/I_{ds} (a figure of merit of device efficiency) is 1.5–2 mS/mA. Typical power FET values for g_m/I_{ds} are 0.7–1 mS/mA. Thus, these devices are expected to be very efficient. In addition, within the limit of a spike-doped layer, MESFET third-order intermodulation is significantly reduced; i.e., for a given level of distortion, a pulse-doped FET should have higher output power and

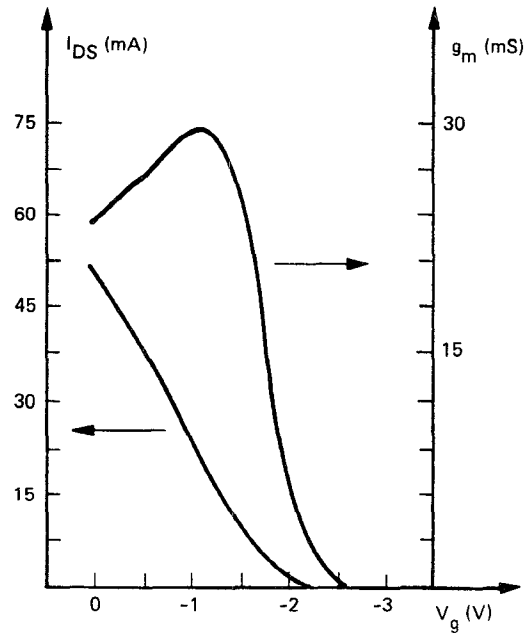


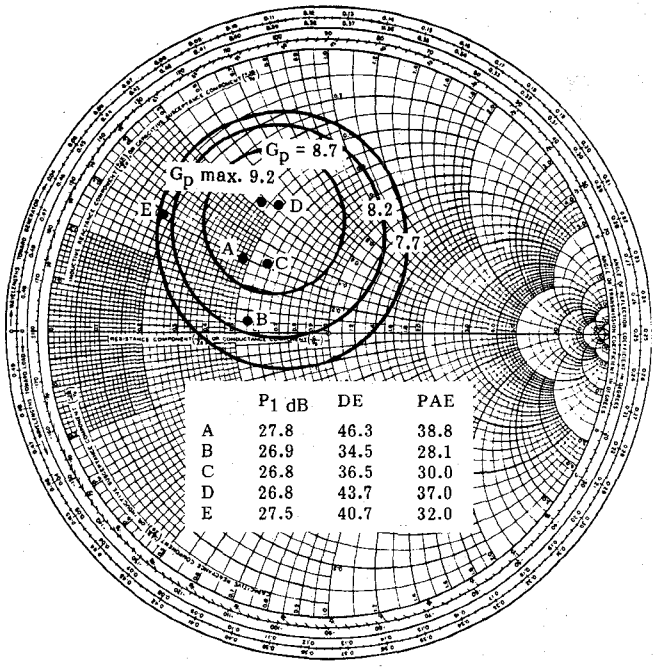
Fig. 3. dc transfer curve of a 0.5 μm×200 μm test MESFET. Plotted I_{ds} and g_m versus V_g for $V_{ds} = 9.0$ V.

efficiency than a FET fabricated on a conventional constant-doped active layer [4].

The next step in obtaining design information is to determine the quiescent drain current and the voltage at which the device provides power most efficiently. Considering the drain current first, drain efficiency is expected to increase with decreasing drain current (going from class A to class B bias). However, the lowest current bias may not provide the best PAE because PAE depends on gain, and gain generally falls off with lower current bias. This is particularly true for MESFET's operating in X-band and above, which may have less than 6 dB of small-signal gain left at 10% I_{dss} current bias.

Considering drain voltage, both drain and power-added efficiency as well as output power are expected to rise with increasing drain voltage until the point where the large-signal RF voltage swing is limited by the gate–drain breakdown voltage. Both drain and power-added efficiency rise, since gain is not a strong function of drain voltage. From the point where the voltage swing becomes limited, output power and efficiency decrease with increasing drain voltage.

The method used to find the bias for best PAE involved making a combination of S-parameter and load-pull measurements. First, loads for maximum 1 dB compressed power were measured with a load pull at 11 GHz for drain voltages of 7, 8, and 9 V with quiescent currents of 50, 30, 20, and 10% of I_{dss}. Both the output powers and drain efficiencies were noted. (In the load-pull measurement system, harmonics were resistively terminated through pads beyond the drain tuner.) Using S-parameter data measured at these same bias points, gains at the loads for maximum power were found using Super-Compact. Using the gains and drain efficiencies, power-added



	$P_{1\,dB}$	DE	PAE
A	27.8	46.3	38.8
B	26.9	34.5	28.1
C	26.8	36.5	30.0
D	26.8	43.7	37.0
E	27.5	40.7	32.0

Fig. 4. Gain circles and load-pull points at 9.0 GHz for the 1200 μm MESFET. Included are compressed power ($P_{1\,dB}$ in dBm), drain efficiency (DE in %), and power-added efficiency (PAE in %) data.

efficiencies were calculated. The bias having best PAE at maximum power was found to be a drain voltage of 9 V at a quiescent current of 20% of I_{dss}.

Using this bias, the value of the load for best power-added efficiency was sought. To find it, a more extensive load-pull measurement was done to generate power/drain efficiency points at 8, 9, 10, and 11 GHz. The power/drain efficiency points in conjunction with the gain circles were used to calculate PAE points. Fig. 4 shows a Smith chart plot of gain circles and power/efficiency points at 9 GHz for the MESFET. These points were used to select the load providing best efficiency over the frequency band.

On the Smith chart, the maximum measured power/drain efficiency point was near the maximum gain point. This condition is characteristic of a device with high PAE because PAE is proportional to both drain efficiency (DE) and gain (G), as shown by the well-known relation

$$\mathrm{PAE} = \mathrm{DE} \times (1 - 1/G).$$

Having found the fundamental frequency load, the second-harmonic load was added to the unit cell design to enhance efficiency. Previous investigators [5], [6] have shown enhancements from 5% to 15% with this technique. Termination of only the second harmonic is an abbreviation of the method outlined by Snider [7] of terminating all of the harmonics. He showed that, in theory, conventional class B operation modified by terminating the even harmonics with short circuits and odd harmonics in open circuits results in drain efficiencies that approach 100% in the limit. This limit is significantly better than the conventional class B limit of 78%, which assumes all harmonics are resistively terminated.

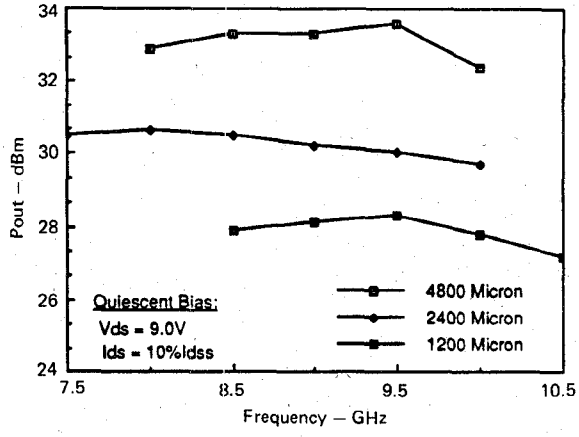


Fig. 5. Output power of 1200, 2400, and 4800 μm amplifiers.

A short to the second harmonic at the drain terminal of the FET was provided using a quarter-wave shorted stub at the center of the fundamental band. Simulation predicted that this presented a low impedance load with phase of $180° \pm 45°$ in the second-harmonic band without significantly affecting the fundamental load presented. To increase reinjection of the second harmonic, an additional fundamental quarter-wavelength short was provided at a harmonic half-wavelength further in the output match.

In order to obtain larger output power levels, unit cells were combined. Of concern is the amount of efficiency lost in output power combining. To investigate this, the 1200 μm unit cell was combined with one and two levels of Wilkinson combiners (chosen for their potential of providing low loss in a modest bandwidth) including an isolation resistor to realize 2400 μm and 4800 μm gate periphery single-stage amplifiers, respectively (see parts (b) and (c) of Fig. 1). The 4800 μm amplifier was fabricated in a way which allowed the direct measurement of the insertion loss of the last combining stage.

A potential problem characteristic of combined power amplifiers is the possibility for odd-mode oscillation. Freitag *et al.* [8] shows in detail how large MESFET's separated by a certain electrical length can oscillate. Odd-mode oscillations occur because the FET is unstable to a short circuit, which the odd-mode circuit provides at the plane of symmetry between two unit cells.

As an alternative to the Freitag solution, the MESFET's of the 1200 μm amplifiers were stabilized at those frequencies of potential instability by adding a shunt resistor of 250 Ω to the gate through a shorting capacitor. Very little degradation in gain was observed in the model with this additional element. With the 1200 μm amplifiers unconditionally stable in and out of band, the larger amplifiers would not oscillate.

III. Results

The power-added efficiencies achieved for the 1200, 2400, and 4800 μm amplifiers are significantly better than any of the narrower-band power amplifiers of comparable power level in X-band reported to date (see Figs. 5 and 6). The recorded bands for the combined amplifiers are

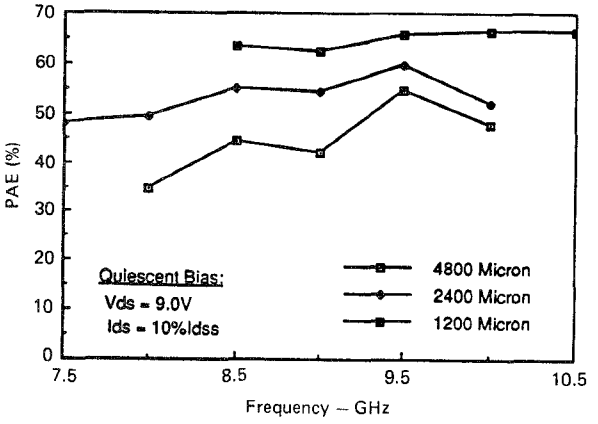


Fig. 6. Power-added efficiency (PAE) of 1200, 2400, and 4800 μm amplifiers.

TABLE I
AVERAGE VALUES OF EFFICIENCY AND OUTPUT POWER (P_{1dB}) FOR 1200, 2400, AND 4800 μm AMPLIFIERS (QUIESCENT BIAS: $V_{ds} = 9.0$ V, $I_{ds} = 10\%\ I_{dss}$)

Amplifier	Average PldB (dBm)	Average Drain Efficiency (%)	Average PAE (%)
1200 micron	27.8	83	65
2400 micron	30.2	72	52
4800 micron	33.1	67	45

0.5 GHz lower in frequency than the 1200 μm amplifier, due to inaccuracies in the first iteration combining structure.

Table I shows a comparison of the average values of power and efficiency of the three amplifiers. The average drain efficiencies decreased 10% and 15% with added levels of combining. This reduction corresponds to an average of 0.5 dB loss in output power per combining stage, given the average drain efficiency of 83% for the 1200 μm unit cell. The estimate of power lost using drain efficiency reduction agrees with the average measured insertion loss of the last stage of combining of 0.8 dB in band. This corresponds to an average of 0.4 dB loss in power per level of combining.

Table II shows the measured powers of the 2400 μm amplifier with the isolation resistors in place and with the isolation resistor in the drain combiner removed. The results for the isolated and nonisolated conditions show no significant difference when compared to the general repeatability of the compression measurements (0.2 dBm for power and 2% for PAE). The insignificance of the isolation shows that the FET's, chosen on the basis of similar dc parameters, appear to be well matched. They were selected on the basis of their similar pinch-off voltage, I_{dss}, transconductance, and gate capacitance.

Fig. 7 shows the differing efficiencies of the 2400 μm amplifier as small-signal current bias is varied from 10% I_{dss} to 30% I_{dss}. While output power is comparable at all

TABLE II
POWER PERFORMANCE OF 2400 μm AMPLIFIER WITH AND WITHOUT ISOLATION RESISTOR IN DRAIN COMBINER

Frequency (GHz)	PldB (dBm)		PAE (%)	
	Isolated	Non-Isolated	Isolated	Non-Isolated
8.5	30.3	30.3	55	56
9.0	30.1	29.9	55	52
9.5	29.8	29.8	60	59
10.0	29.4	29.7	50	53

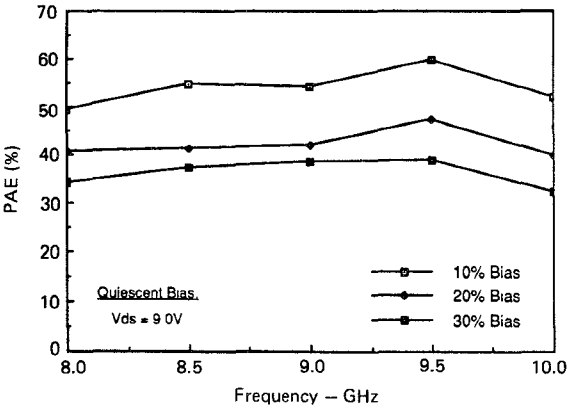


Fig. 7. Effect of quiescent current bias on efficiency for 2400 μm amplifier.

three bias levels, the average PAE has decreased 10% in going from 10% to 20% current bias and another 6% in going to 30% current bias.

IV. DISCUSSION

The average drain efficiency over the band of the noncombined 1200 μm amplifier (83%) exceeded the theoretical maximum of 78% for a conventional class B amplifier with resistive termination of all harmonics. This suggests that a perfect short throughout the second-harmonic band is not required. General improvement in efficiency beyond conventional class B operation is achieved with any low-impedance harmonic load with a very small resistive component.

The significant improvements in power-added efficiency as the current bias is decreased from 30% to 10% I_{dss} are possible only because the MESFET provides small-signal gain greater than 7 dB at 10% current bias. This feature, in addition to retaining adequate power levels at the low bias, enables the device to take full advantage of harmonically terminated class AB operation.

It should be noted that the bias suggested by the load-pull measurement for best PAE was different from that measured for the amplifier ($V_{ds} = 9$ V, $I_{ds} = 10\%\ I_{dss}$). This difference suggests that the load-pull measurement could be enhanced by providing the second harmonic with a low-loss, low-impedance termination. Since the phasing of the termination is not critical, an alumina circuit containing a quarter-wave short at the fundamental frequency can be inserted before the drain tuner to

enhance the measurement by providing a known load to the second harmonic.

The effects of combiners and combiner isolation on efficiency have been measured. The degradation in efficiency appeared to be caused by the average 0.5 dB insertion loss of the combiners, as opposed to differences in parallel FET's. If the 0.2 dB loss per stage estimated in [9] for Wilkinson combiners is achieved in these amplifiers, 4% degradation in drain efficiency per stage can be expected.

Experiment has shown no need for drain combiner isolation to aid output power and efficiency if devices for hybrid amplifiers are selected for matched dc parameters. It is anticipated that a MMIC amplifier will also not require combiner isolation, since the FET's of a particular amplifier are expected to be matched because of their proximity. The requirement for gate-divider isolation was not assessed because upon removing the gate-isolation resistor, the combined amplifier oscillated. The oscillation occurred with no RF input. It is believed that the shunt RC suppression circuit which worked at the designed 20% I_{dss} bias did not provide a low enough shunt resistance for the lower 10% current bias.

After considering the issues involved in designing efficient power amplifiers, it is clear that the most efficient power amplifiers in X-band and above will be made with power FET's which have been improved along two fronts. The need for increased power per unit FET periphery is commonly understood. In addition, to take full advantage of harmonic loading, the FET's must provide reasonable gain at 5% or 10% I_{dss} quiescent current bias.

V. Conclusions

X-band 0.5, 1, and 2 W power amplifiers have been presented which exhibit average power-added efficiencies of 65%, 53%, and 45%, respectively. Four issues pertinent to efficient power amplifiers have been emphasized. The drain efficiency of the harmonically terminated 0.5 W amplifier (83%) has shown improvement beyond the conventional class B amplifier limit. The marked dependance of power-added efficiency on bias has been measured, and the requirement for high gain at low current bias highlighted. Amplifier measurements were presented which show efficiency as a function of output power combining. Finally, isolation in output power combining has been shown experimentally to be unimportant when FET's for the amplifier are matched according to dc parameters.

Acknowledgment

The authors would like to express their gratitude to Dr. R. Froelich and Dr. R. Remba for their technical discussions during the project's development and for their comments on the content of the manuscript. They would also like to thank P. Golf for the extensive measurements he made on the amplifiers.

References

[1] T. Tan, K. Kotzebue, D. Braun, J. Centanni, and D. McQuate, "A Low-distortion K-band GaAs power FET," *IEEE Trans. Microwave Theory Tech.*, vol. 36, p. 1023, 1988.

[2] B. D. Cantos and R. D. Remba, "An improved technique for 1/4 micrometer gate length GaAs MESFET fabrication by optical lithography," *SPIE Proc.*, vol. 774, p. 61, 1987.

[3] B. D. Cantos and R. D. Remba, "A reliable method for 0.25-micron gate MESFET fabrication using optical photolithography," *J. Electrochem. Soc.*, vol. 135, p. 1311, 1988.

[4] R. A. Pucel, "Profile design for distortion reduction in microwave field-effect transistors," *Electron. Lett.*, vol. 14, p. 204, 1978.

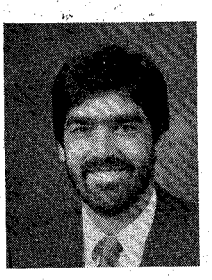
[5] S. Lesage, J. Detra, and J. Beyer, "Optimizing the power-added efficiency of a class B GaAs FET amplifier," in *1988 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 339–342.

[6] B. Kopp and D. Heston, "High-efficiency 5-watt power amplifier with harmonic tuning," in *1988 IEEE MTT Int. Microwave Symp. Dig.*, pp. 839–842.

[7] D. Snider, "A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifier," *IEEE Trans. Electron Devices.*, vol. ED-14, pp. 851–867, Dec. 1967.

[8] R. Freitag, S. Lee, D. Krafcsik, D. Dawson, and J. Degenford, "Stability and improved circuit modeling considerations for high power MMIC amplifiers," in *1988 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 175–178.

[9] J. Komiak "Power combining methods with amplifier design and matching considerations," in *1988 IEEE MTT-S Int. Microwave Symp. Workshop*, paper M-2.



Ronald D. Boesch (S'85–M'86) was born in Quantico, VA, in 1963. He received the B.S. and M.S. degrees in electrical engineering from the University of Illinois in 1985 and 1987, respectively. His graduate work focused on the development of an analog phase shifter for a microwave phased array hyperthermia system.

He joined the Watkins-Johnson Company, Palo Alto, CA, in 1987, where he is responsible for the development of microwave components for subsystem applications in the Subsystems R&D Department. In this role he has developed slope equalizers, N-way power combiners, switches, limiters, filters, and power amplifiers.

Joyce A. Thompson (S'84–M'85) received the B.S. and M.S. degrees from the Massachusetts Institute of Technology in 1980. She received the Ph.D. degree from Stanford University in 1985.

Her responsibilities at the Watkins-Johnson Company, Palo Alto, CA, were for the development and improvement of GaAs power FET devices. She also investigated the stress properties of the materials used to produce FET's and monolithic devices. In addition, she provided technical support for the GaAs production effort. In 1989, Ms. Thompson moved to Bangkok, Thailand, where she has started a company, called TEMAC, which is in the business of failure analysis.